



US 20120075363A1

(19) **United States**(12) **Patent Application Publication**
Kim(10) **Pub. No.: US 2012/0075363 A1**(43) **Pub. Date: Mar. 29, 2012**(54) **PIXEL AND ORGANIC LIGHT EMITTING
DISPLAY USING THE SAME**(52) **U.S. CL. 345/691; 257/88; 257/E51.018;
345/77**(76) **Inventor: Hyung-Soo Kim, Yongin-city (KR)**(21) **Appl. No.: 13/118,149**(22) **Filed: May 27, 2011**(30) **Foreign Application Priority Data**

Sep. 29, 2010 (KR) 10-2010-0094226

Publication Classification(51) **Int. Cl.****G09G 3/32** (2006.01)**G09G 5/10** (2006.01)**H01L 51/52** (2006.01)(57) **ABSTRACT**

A pixel of an organic light emitting display in which the pixel includes: a first transistor including a first electrode coupled to a first power source, a second electrode, and a gate electrode coupled to a first node; a second transistor including a first electrode coupled to a third power source, a second electrode coupled to the first node, and a gate electrode coupled to a reset control line; a third transistor including a first electrode coupled to the first node, a second electrode coupled to a fourth power source, and a gate electrode; a fourth transistor including a first electrode coupled to the gate electrode of the third transistor, a second electrode coupled to a scan line, and a gate electrode coupled to a data line; and an organic light emitting diode (OLED) including an anode electrode coupled to the second electrode of the first transistor, and a cathode electrode coupled to a second power source.

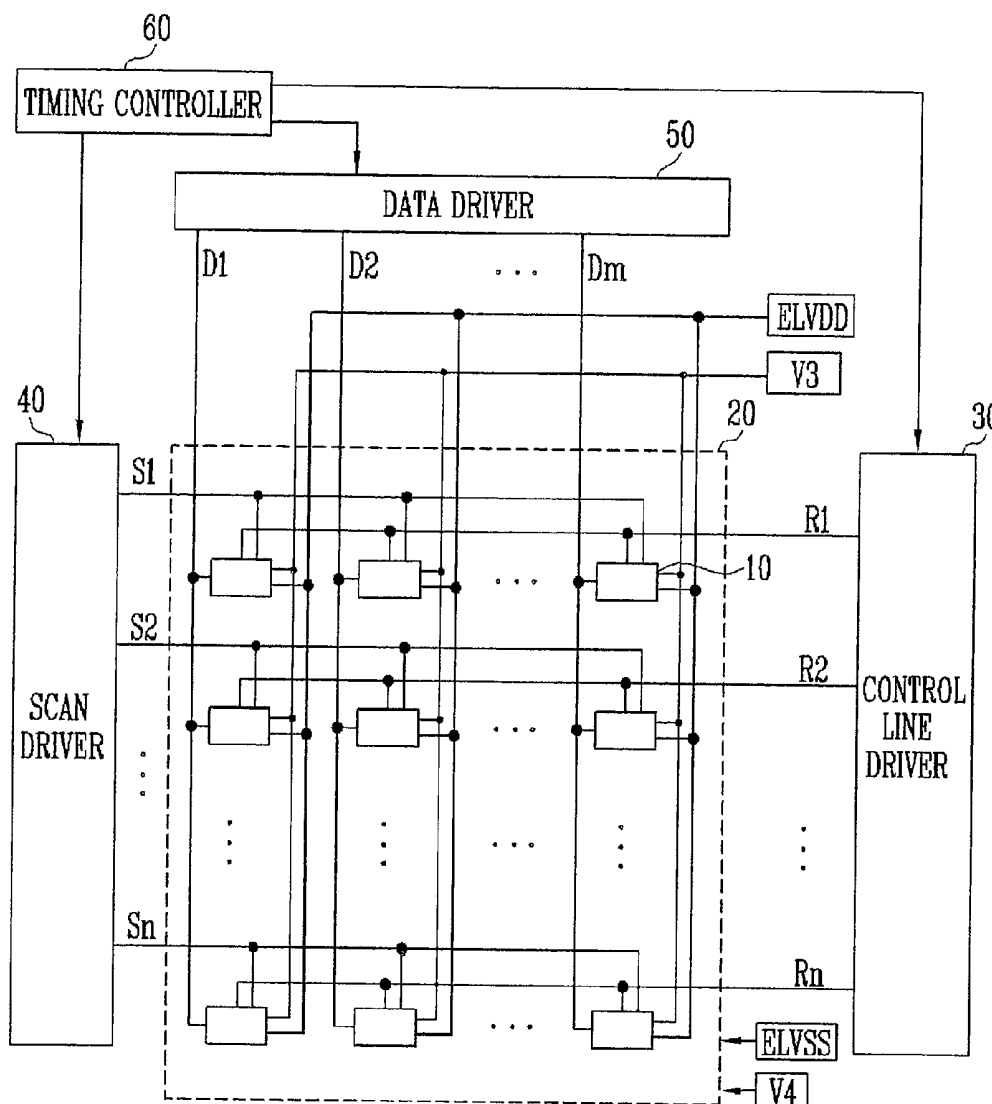


FIG. 1

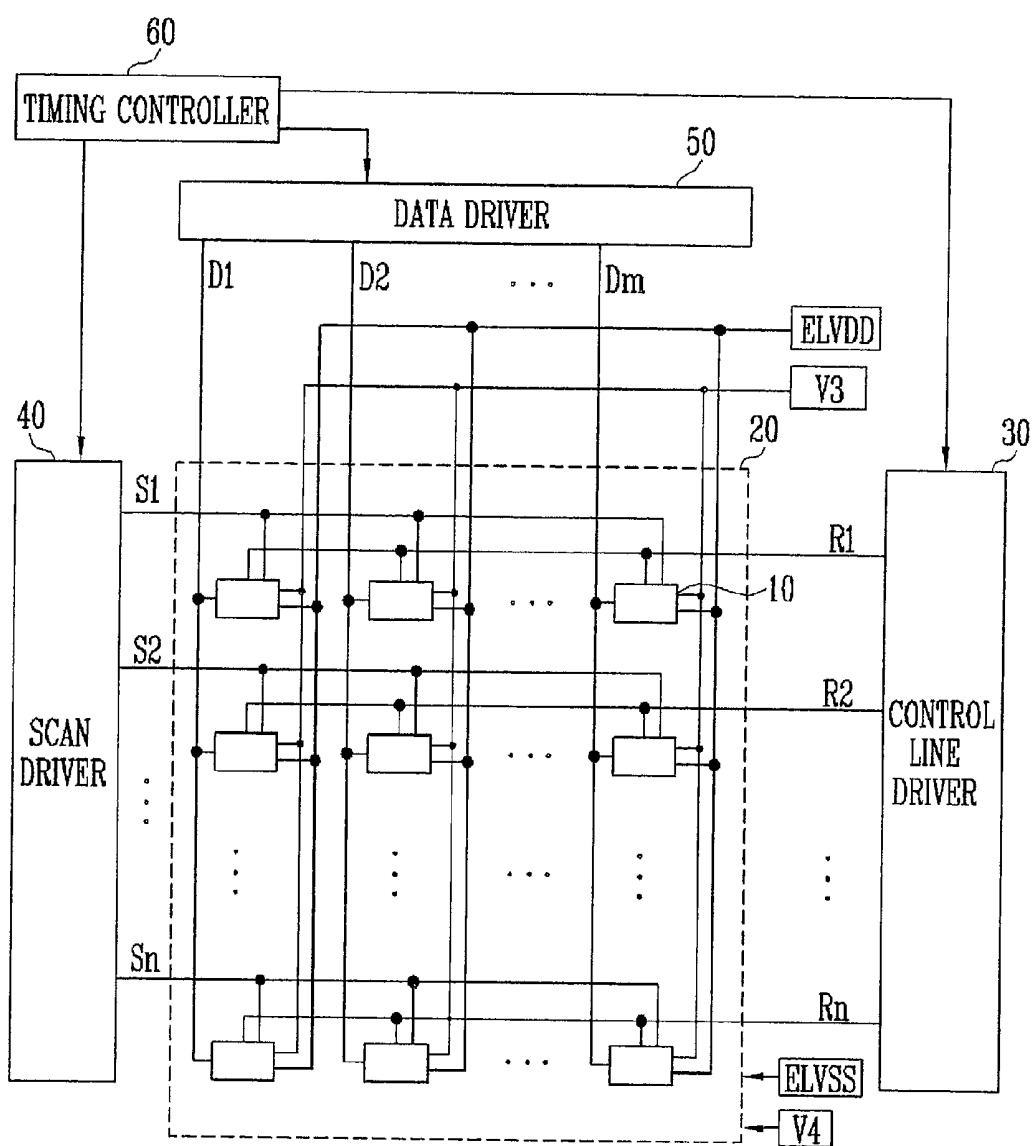


FIG. 2

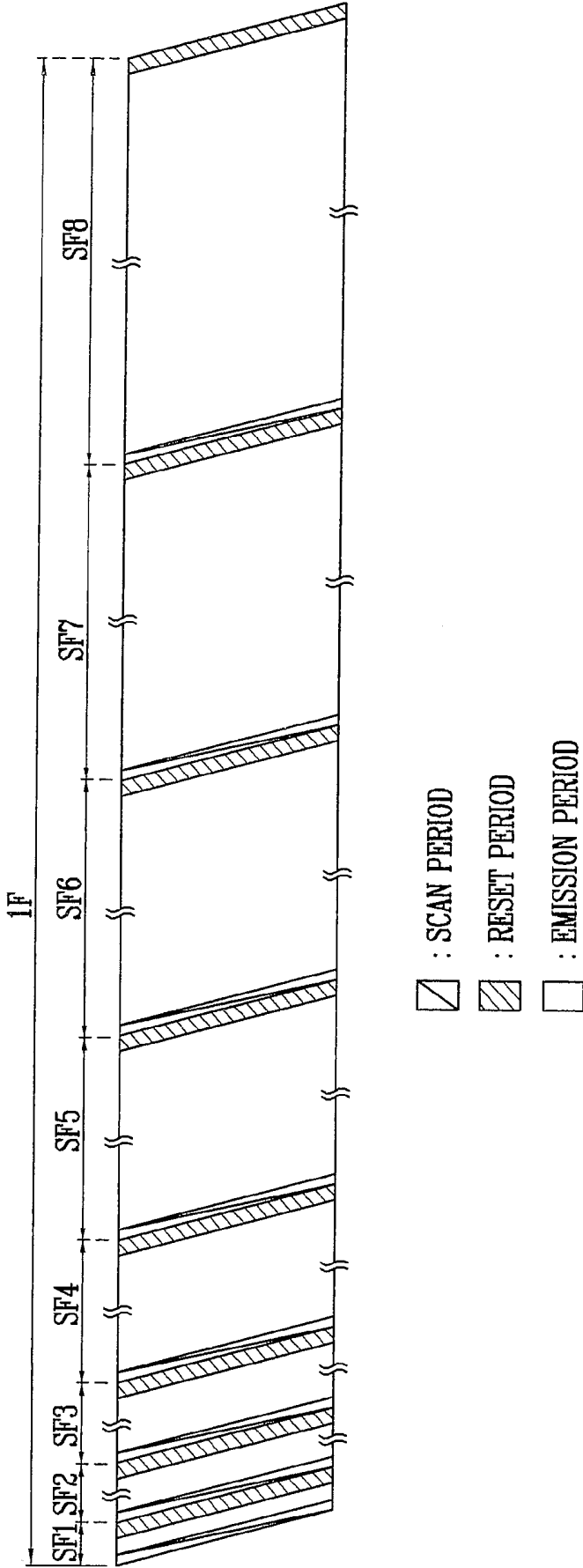


FIG. 3

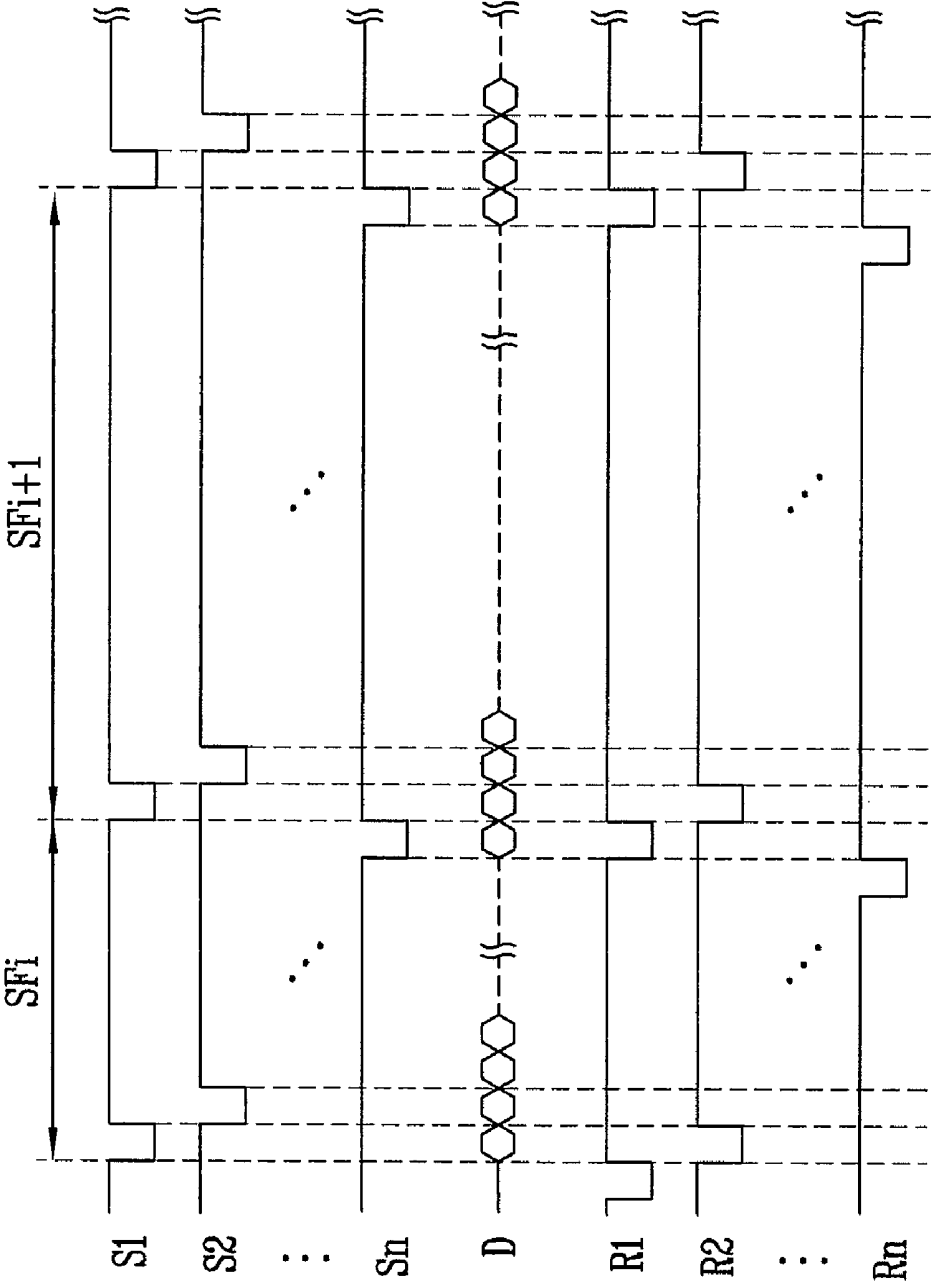


FIG. 4

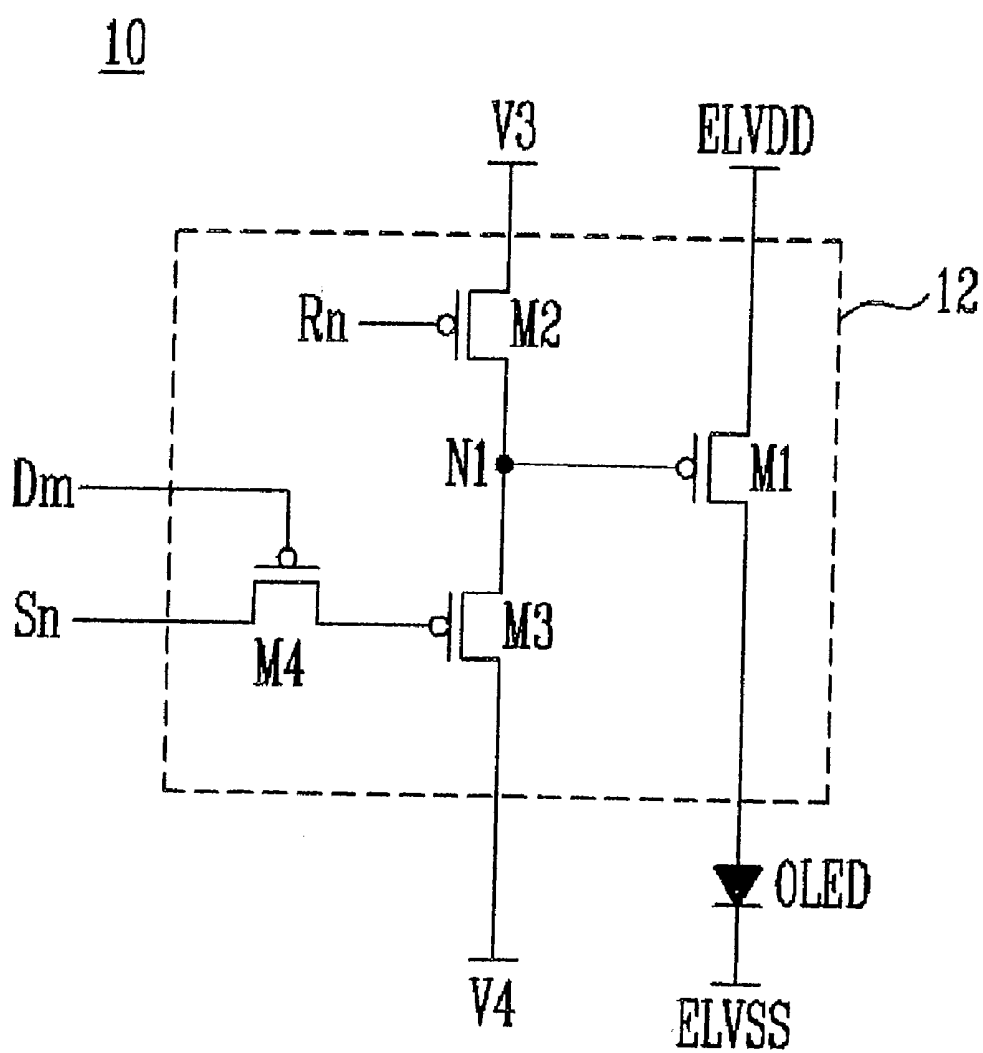


FIG. 5

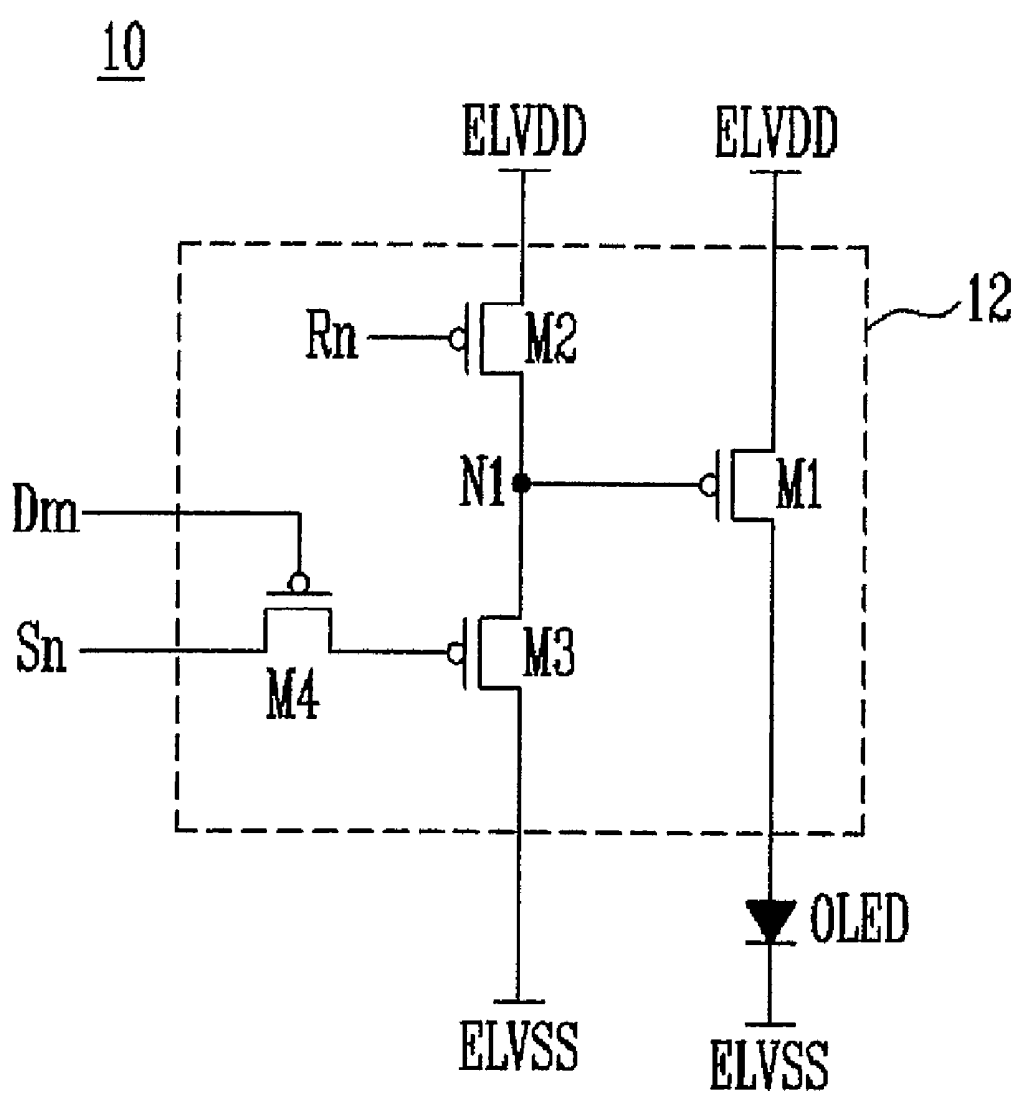
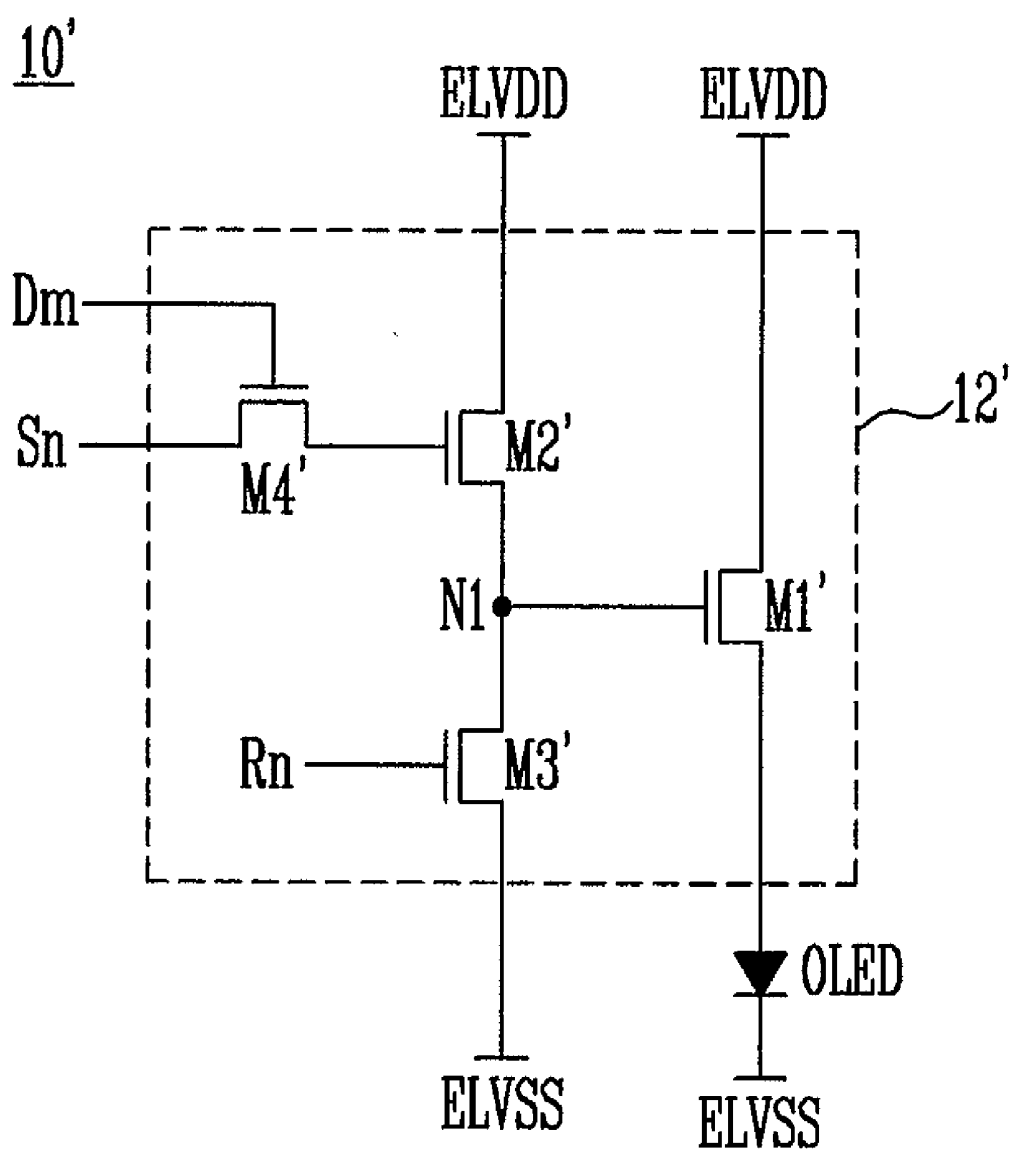


FIG. 6



PIXEL AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2010-0094226, filed on Sep. 29, 2010, in the Korean Intellectual Property Office, the entire content of which is incorporated herein by reference.

BACKGROUND

[0002] 1. Field

[0003] The present invention relates to a pixel and an organic light emitting display using the same.

[0004] 2. Description of Related Art

[0005] Recently, various flat panel displays (FPDs) capable of reducing weight and volume that are disadvantages of cathode ray tubes (CRTs) have been developed. FPDs include liquid crystal displays (LCDs), field emission displays (FEDs), plasma display panels (PDPs), and organic light emitting displays.

[0006] Among the FPDs, organic light emitting displays display an image using organic light emitting diodes (OLEDs) that generate light by recombination of electrons and holes. Organic light emitting displays have high response speed and are driven with low power consumption.

[0007] However, since the pixels of conventional organic light emitting displays display gray scales (e.g., gray levels) using the voltage stored in a storage capacitor, it may be difficult to correctly display desired gray levels (e.g., in analog driving). Since a plurality of gray levels are to be displayed using a uniform voltage that may be stored in the storage capacitor, it may be difficult to correctly display a difference in brightness between adjacent gray levels.

[0008] In addition, when the storage capacitor is used for each of the pixels, for charge/discharge operations of the storage capacitor, time (e.g., predetermined time) is spent so that driving speed is reduced. Furthermore, when the storage capacitor is used for each of the pixels, high power consumption occurs as a result of the charge/discharge of the storage capacitor.

SUMMARY

[0009] Accordingly, embodiments of the present invention provide a pixel capable of reducing power consumed during driving, and capable of performing high speed driving, and an organic light emitting display using the same.

[0010] In order to achieve the foregoing and/or other aspects of embodiments of the present invention, there is provided a pixel including: a first transistor including a first electrode coupled to a first power source, a second electrode, and a gate electrode coupled to a first node; a second transistor including a first electrode coupled to a third power source, a second electrode coupled to the first node, and a gate electrode coupled to a reset control line; a third transistor including a first electrode coupled to the first node, a second electrode coupled to a fourth power source, and a gate electrode; a fourth transistor including a first electrode coupled to the gate electrode of the third transistor, a second electrode coupled to a scan line, and a gate electrode coupled to a data line; and an organic light emitting diode (OLED) including an

anode electrode coupled to the second electrode of the first transistor, and a cathode electrode coupled to a second power source.

[0011] A voltage of the third power source may be substantially the same as a voltage of the first power source.

[0012] A voltage of the fourth power source may be substantially the same as a voltage of the second power source.

[0013] The transistors may be PMOS transistors or NMOS transistors.

[0014] According to another embodiment of the present invention, there is provided an organic light emitting display including a scan line driver for sequentially supplying scan signals to scan lines in scan periods in a plurality of sub frames of one frame, a control line driver for sequentially supplying reset signals to reset control lines in reset periods in the sub frames, a data driver for supplying data signals to data lines in the scan periods, and a display unit including pixels configured to emit light in emission periods in the sub frames, and configured to be transitioned into a non-emission state to not emit light in a reset period of the reset periods, wherein each of the pixels includes: a first transistor including a first electrode coupled to a first power source, a second electrode, and a gate electrode coupled to a first node; a second transistor including a first electrode coupled to a third power source, a second electrode coupled to the first node, and a gate electrode coupled to a reset control line of the reset control lines; a third transistor including a first electrode coupled to the first node, a second electrode coupled to a fourth power source, and a gate electrode; a fourth transistor including a first electrode coupled to the gate electrode of the third transistor, a second electrode coupled to a scan line of the scan lines, and a gate electrode coupled to a data line of the data lines; and an OLED including an anode electrode coupled to the second electrode of the first transistor, and a cathode electrode coupled to a second power source.

[0015] A voltage of the third power source may be substantially the same as a voltage of the first power source.

[0016] A voltage of the fourth power source may be substantially the same as a voltage of the second power source.

[0017] The transistors may be PMOS transistors or NMOS transistors.

[0018] As described above, according to embodiments of the present invention, the pixel capable of reducing power consumed during driving, and capable of performing high speed driving, and the organic light emitting display using the same may be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The accompanying drawings, together with the specification, illustrate exemplary embodiments of the present invention, and, together with the description, serve to explain principles and aspects of embodiments of the present invention.

[0020] FIG. 1 is a view illustrating an organic light emitting display according to a first embodiment of the present invention;

[0021] FIG. 2 is a view illustrating one frame according to an embodiment of the present invention;

[0022] FIG. 3 is a view illustrating driving waveforms supplied in a sub frame period included in one frame according to an embodiment of the present invention;

[0023] FIG. 4 is a view illustrating a pixel according to the first embodiment of the present invention;

[0024] FIG. 5 is a view illustrating a pixel according to a second embodiment of the present invention; and

[0025] FIG. 6 is a view illustrating a pixel according to a third embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Hereinafter, certain exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being coupled to a second element, the first element may be directly coupled to the second element or may be indirectly coupled to the second element via one or more other elements. Further, some of the elements that are not essential to a complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0027] Specific items of the other embodiments are included in the detailed description and drawings.

[0028] The aspects of embodiments of the present invention, and a method of achieving the aspects of embodiments of the present invention, will be clarified with reference to the embodiments described hereinafter in detail together with the accompanying drawings. However, the present invention is not limited to the embodiments disclosed hereinafter, but may be realized in different forms without departing from the spirit and scope of the present invention.

[0029] FIG. 1 is a view illustrating an organic light emitting display according to a first embodiment of the present invention.

[0030] Referring to FIG. 1, the organic light emitting display according to the first embodiment of the present invention includes a display unit 20 including: a plurality of pixels 10 coupled to scan lines S1 to Sn, reset control lines R1 to Rn, data lines D1 to Dm, a first power source ELVDD, a second power source ELVSS, a third power source V3, and a fourth power source V4; a control line driver 30 for supplying reset signals to the pixels 10 through the reset control lines R1 to Rn; a scan driver 40 for supplying scan signals to the pixels 10 through the scan lines S1 to Sn; and a data driver 50 for supplying data signals to the pixels 10 through the data lines D1 to Dm. The organic light emitting display may further include a timing controller 60 for controlling the control line driver 30, the scan driver 40, and the data driver 50.

[0031] The data driver 20 supplies the data signals to the data lines D1 to Dm in each of a plurality of sub frames included in one frame. Here, the data signals are divided into first data signals by which the pixels 10 may emit light, and second data signals by which the pixels 10 do not emit light.

[0032] The data driver 20 supplies the first data signals or the second data signals for controlling whether the pixels 10 emit light to the data lines D1 to Dm in each of the sub frames.

[0033] The scan driver 10 sequentially supplies the scan signals to the scan lines S1 to Sn in each of the sub frames. When the scan signals are sequentially supplied to the scan lines S1 to Sn, the pixels 10 are sequentially selected by lines (e.g., line by line), and the selected pixels 10 receive the first data signals or the second data signals supplied from the data lines D1 to Dm.

[0034] The control line driver 30 sequentially supplies the reset signals to the reset control lines R1 to Rn after the pixels 10 emit light for an amount of time (e.g., a predetermined time) in the sub frames.

[0035] The pixels 10 that receive the reset signals are in or transitioned into a non-emission state regardless of a previous state.

[0036] The display unit 20 receives power from the first power source ELVDD, the second power source ELVSS, the third power source V3, and the fourth power source V4 from the outside (e.g., from sources external to the display unit 20) to supply power from the first power source ELVDD, the second power source ELVSS, the third power source V3, and the fourth power source V4 to the pixels 10.

[0037] The pixels 10 that receive power from the first power source ELVDD, the second power source ELVSS, the third power source V3, and the fourth power source V4 receive the data signals (the first data signals or the second data signals) when the scan signals are supplied, and emit light or do not emit light in the sub frames in accordance with the received data signals. The pixels 10 are transitioned into a non-emission state using a voltage of the third power source V3 when the reset signals are supplied.

[0038] FIG. 2 is a view illustrating one frame according to an embodiment of the present invention. FIG. 3 is a view illustrating driving waveforms supplied in a sub frame period included in one frame.

[0039] Referring to FIGS. 2 and 3, one frame 1F of the described embodiment of the present invention is divided into a plurality of sub frames SF1 to SF8 to be driven (e.g., digital driving).

[0040] The sub frames SF1 to SF8 are divided into a scan period for sequentially supplying the scan signals, an emission period in which the pixels 10 that receive the first data signals in the scan period emit light, and a reset period in which the pixels 10 are transitioned into the non-emission state to be driven.

[0041] In the scan period, the scan signals are sequentially supplied to the scan lines S1 to Sn, and the first data signals or the second data signals are supplied to the data lines D1 to Dm. That is, in the scan period, the pixels 10 receive the first data signals or the second data signals.

[0042] In the emission period, the pixels 10 maintain the first data signals and the second data signals supplied in the scan period to emit light or to not emit light. That is, the pixels 10 that receive the first data signals in the scan period are set in the emission state in the corresponding sub frame period, and the pixels 10 that receive the second data signals are set in the non-emission state in the corresponding sub frame period.

[0043] Here, for example, the emission periods of the sub frames SF1 to SF8 are set to vary. For example, when an image is to be displayed by 256 gray levels, as illustrated in FIG. 2, one frame is divided into eight sub frames SF1 to SF8. The emission periods of the eight sub frames SF1 to SF8 increase in the ratio of 2^n ($n=0, 1, 2, 3, 4, 5, 6$, and 7).

[0044] That is, according to embodiments of the present invention, whether the pixels 10 emit light is controlled in the sub frames (e.g., SF1 to SF8) to display an image of a gray level (e.g., a predetermined gray level). That is, according to embodiments of the present invention, a gray level (e.g., a predetermined gray level) is displayed in one frame 1F period corresponding to the sum of times for which the pixels 10 emit light in the sub frame periods.

[0045] One frame 1F illustrated in FIG. 2 is an example for displaying according to embodiments of the present invention, and the present invention is not limited to the above. For

example, one frame 1F may be divided into 10 sub frames or more, and the emission periods of the sub frames may be varied.

[0046] In the reset period, the reset signals are sequentially supplied to the reset control lines R1 to Rn. Actually, the reset signals are supplied to the pixels 10 after the pixels 10 emit light for an amount of time (e.g., a predetermined time) in the sub frames (e.g., SF1 to SF8). For example, the reset signal supplied to the i^{th} (i is a natural number) reset control line Ri may be supplied immediately before a scan signal supplied to the i^{th} scan line Si, as illustrated in FIG. 3. When the reset signals are sequentially supplied to the reset control lines R1 to Rn in the reset period, the pixels 10 are sequentially transitioned into the non-emission state.

[0047] FIG. 4 is a view illustrating a pixel according to the first embodiment of the present invention. In FIG. 4, for convenience's sake, the pixel 10 coupled to the n^{th} scan line Sn and the m^{th} data line Dm will be illustrated.

[0048] Referring to FIG. 4, the pixel 10 according to the first embodiment of the present invention includes a pixel circuit 12 coupled to an organic light emitting diode OLED, the data line Dm, the reset control line Rn, and the scan line Sn, to control the OLED.

[0049] An anode electrode of the OLED is coupled to the pixel circuit 12 and a cathode electrode of the OLED is coupled to the second power source ELVSS. Whether the OLED emits light is controlled in accordance with a data signal supplied to the pixel circuit 12.

[0050] The pixel circuit 12 controls whether the OLED emits light according to the data signal supplied to the data line Dm when a scan signal is supplied to the scan line Sn. The pixel circuit 12 receives power from the third power source V3 when a reset signal is supplied to the reset control line Rn to transit the OLED into the non-emission state.

[0051] Therefore, the pixel circuit 12 includes first to fourth transistors M1, M2, M3, and M4.

[0052] A first electrode of the first transistor M1 is coupled to the first power source ELVDD, a second electrode of the first transistor M1 is coupled to the anode electrode of the OLED, and a gate electrode of the first transistor M1 is coupled to a first node N1. The first transistor M1 is turned on or turned off according to the voltage value applied to the first node N1 to control the emission or non-emission of the OLED.

[0053] A first electrode of the second transistor M2 is coupled to the third power source V3, a second electrode of the second transistor M2 is coupled to the first node, and a gate electrode of the second transistor M2 is coupled to the reset control line Rn. The second transistor M2 is turned on when the reset signal is supplied to the reset control line Rn to apply power from the third power source V3 to the first node N1.

[0054] The reset signal for turning on the second transistor M2 has a low level voltage when the second transistor M2 is a PMOS transistor, as illustrated in FIG. 4, and has a high level voltage when the second transistor M2 is an NMOS transistor.

[0055] A first electrode of the third transistor M3 is coupled to the first node N1, a second electrode of the third transistor M3 is coupled to the fourth power source V4, and a gate electrode of the third transistor M3 is coupled to a first electrode of the fourth transistor M4. The third transistor M3 is turned on to apply power from the fourth power source V4 to

the first node N1 when a scan signal transmitted by the fourth transistor M4 is supplied to the gate electrode of the third transistor M3.

[0056] The first electrode of the fourth transistor M4 is coupled to the gate electrode of the third transistor M3, a second electrode of the fourth transistor M4 is coupled to the scan line Sn, and a gate electrode of the fourth transistor M4 is coupled to the data line Dm.

[0057] The fourth transistor M4 is turned on to apply the scan signal supplied to the scan line Sn to the gate electrode of the third transistor M3 when the first data signals are supplied from the data line Dm. When the second data signals are supplied from the data line Dm, the fourth transistor M4 is turned off to block the transmission of the scan signal.

[0058] The first data signals for turning on the fourth transistor M4 have low level voltages when the fourth transistor M4 is a PMOS transistor, as illustrated in FIG. 4, and have high level voltages when the fourth transistor M4 is an NMOS transistor.

[0059] The second data signals for turning off the fourth transistor M4 have high level voltages when the fourth transistor M4 is a PMOS transistor, as illustrated in FIG. 4, and have low level voltages when the fourth transistor M4 is an NMOS transistor.

[0060] The first power source ELVDD as a high potential power source is coupled to the first electrode of the first transistor M1.

[0061] The second power source ELVSS as a low potential power source (for example, Ground) (e.g., a potential power source that is lower than the first power source ELVDD) is coupled to the cathode electrode of the OLED.

[0062] The third power source V3 as a high potential power source is applied to the first node N1 when a reset signal is supplied (e.g., to the gate electrode of the second transistor M2) to turn off the first transistor M1. The voltage of the third power source V3 may be set to be the same as a voltage of the first power source ELVDD.

[0063] The fourth power source V4 as a low potential power source is applied to the first node N1 to turn on the first transistor M1 when the scan signal is supplied to turn on the third transistor M3 (e.g., the scan signal is supplied via the fourth transistor M4 to the gate electrode of the third transistor M3). A voltage of the fourth power source V4 may be set to be the same as a voltage of the second power source ELVSS.

[0064] The first node N1 is a contact point at which the gate electrode of the first transistor M1, the second electrode of the second transistor M2, and the first electrode of the third transistor M3 are coupled.

[0065] When an operation process of the pixel 10 according to the first embodiment is described in detail, the scan signal and the data signal are supplied to the pixels 10 in the scan period.

[0066] The data driver 50 supplies the first data signals for the pixels 10 that emit light, and supplies the second data signals to the pixels 10 that do not emit light. This is because, unlike the conventional pixel structure, according to embodiments of the present invention, the data signal is applied to the gate electrode of the fourth transistor M4.

[0067] When the first data signals are supplied to the data line Dm, the fourth transistor M4 is turned on to apply the scan signal to the gate electrode of the third transistor M3.

Therefore, the third transistor M3 is turned on by the scan signal so that power from the fourth power source V4 is applied to the first node N1.

[0068] When power from the fourth power source V4 is applied to the first node N1, since the fourth power source V4 is a low level voltage, the first transistor M1 is turned on. When the first transistor M1 is turned on, current corresponding to the first power source ELVDD is supplied to the OLED. Then, the OLED emits light in the corresponding sub frame period.

[0069] When the second data signals are supplied to the data line Dm, the fourth transistor M4 is turned off to block the transmission of the scan signal to the gate electrode of the third transistor M3. Therefore, the third transistor M3 is not turned on so that power from the fourth power source V4 is not applied to the first node N1.

[0070] As a result, the first transistor M1 is not turned on, and the OLED maintains the non-emission state in the corresponding sub frame period.

[0071] The pixels 10 that receive the first data signals emit light, and a reset period exists after the emission period in which the pixels 10 that receive the second data signals do not emit light.

[0072] In the reset period, the reset signal is supplied to the reset control line Rn, and the second transistor M2 is turned on by the supply of the reset signal. As the second transistor M2 is turned on, power from the third power source V3 is applied to the first node N1.

[0073] Since power from the third power source V3 is a high level voltage, the first transistor M1 is turned off, and the OLED that emits light is transitioned into the non-emission state.

[0074] As described above, according to embodiments of the present invention, one frame (e.g., 1 F) is divided into a plurality of sub frames (e.g., SF1 to SF8), and whether or not the pixels 10 emit light is controlled in the sub frame period to display gray levels. As described above, when the gray levels are displayed corresponding to whether the pixels 10 emit light, a desired gray level may be correctly displayed.

[0075] In addition, when a voltage is applied to the gate electrode of the first transistor M1, since the gate overlap capacitance of the first transistor M1 and the parasitic capacitance of the second transistor M2 and the third transistor M3 exist, an additional storage capacitor is not necessary.

[0076] Since the voltage required for (e.g., applied to) the gate electrode of the first transistor M1 is supplied from the third power source V3 and the fourth power source V4 in a pixel 10, power consumption is reduced, and driving speed also increases.

[0077] FIG. 5 is a view illustrating a pixel according to a second embodiment of the present invention.

[0078] Referring to FIG. 5, the third power source V3 of the first embodiment is changed to the first power source ELVDD in the second embodiment, and the fourth power source V4 of the first embodiment is changed to the second power source ELVSS in the second embodiment.

[0079] That is, the third power source V3 may be the same as the first power source ELVDD, and the fourth power source V4 may be the same as the second power source ELVSS.

[0080] When the above-described changes are made, the above-described operation may be performed, and it is not necessary to include additional third and fourth power sources V3 and V4.

[0081] FIG. 6 is a view illustrating a pixel according to a third embodiment of the present invention. In FIG. 5, the pixel 10 in which the first to fourth transistors M1 to M4 are PMOS transistors is illustrated. However, in FIG. 6, a pixel 10' in which the first to fourth transistors M1, M2', M3', and M4' are NMOS transistors is illustrated.

[0082] While the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, and equivalents thereof.

What is claimed is:

1. A pixel of an organic light emitting display, the pixel comprising:

a first transistor comprising:

- a first electrode coupled to a first power source;
- a second electrode; and
- a gate electrode coupled to a first node;

a second transistor comprising:

- a first electrode coupled to a third power source;
- a second electrode coupled to the first node; and
- a gate electrode coupled to a reset control line;

a third transistor comprising:

- a first electrode coupled to the first node;
- a second electrode coupled to a fourth power source; and
- a gate electrode;

a fourth transistor comprising:

- a first electrode coupled to the gate electrode of the third transistor;

- a second electrode coupled to a scan line; and
- a gate electrode coupled to a data line; and

an organic light emitting diode (OLED) comprising:

- an anode electrode coupled to the second electrode of the first transistor; and
- a cathode electrode coupled to a second power source.

2. The pixel as claimed in claim 1, wherein a voltage of the third power source is substantially the same as a voltage of the first power source.

3. The pixel as claimed in claim 2, wherein a voltage of the fourth power source is substantially the same as a voltage of the second power source.

4. The pixel as claimed in claim 1, wherein the transistors are PMOS transistors or NMOS transistors.

5. An organic light emitting display comprising:

- a scan line driver for sequentially supplying scan signals to scan lines in scan periods in a plurality of sub frames of one frame;
- a control line driver for sequentially supplying reset signals to reset control lines in reset periods in the sub frames;
- a data driver for supplying data signals to data lines in the scan periods; and
- a display unit comprising pixels configured to emit light in emission periods in the sub frames, and configured to be transitioned into a non-emission state to not emit light in a reset period of the reset periods,

wherein each of the pixels comprises:

a first transistor comprising:

- a first electrode coupled to a first power source;
- a second electrode; and
- a gate electrode coupled to a first node;

a second transistor comprising:
a first electrode coupled to a third power source;
a second electrode coupled to the first node; and
a gate electrode coupled to a reset control line of the reset control lines;
a third transistor comprising:
a first electrode coupled to the first node;
a second electrode coupled to a fourth power source; and
a gate electrode;
a fourth transistor comprising:
a first electrode coupled to the gate electrode of the third transistor;
a second electrode coupled to a scan line of the scan lines; and
a gate electrode coupled to a data line of the data lines; and

an OLED comprising:
an anode electrode coupled to the second electrode of the first transistor; and
a cathode electrode coupled to a second power source.

6. The organic light emitting display as claimed in claim 5, wherein a voltage of the third power source is substantially the same as a voltage of the first power source.

7. The organic light emitting display as claimed in claim 6, wherein a voltage of the fourth power source is substantially the same as a voltage of the second power source.

8. The organic light emitting display as claimed in claim 5, wherein the transistors are PMOS transistors or NMOS transistors.

* * * * *

专利名称(译)	使用其的像素和有机发光显示器		
公开(公告)号	US20120075363A1	公开(公告)日	2012-03-29
申请号	US13/118149	申请日	2011-05-27
[标]申请(专利权)人(译)	金亨SOO		
申请(专利权)人(译)	金亨洙		
当前申请(专利权)人(译)	金亨洙		
[标]发明人	KIM HYUNG SOO		
发明人	KIM, HYUNG-SOO		
IPC分类号	G09G3/32 G09G5/10 H01L51/52		
CPC分类号	G09G3/2022 G09G3/3225 H01L27/3244 G09G2310/061 G09G2300/0814		
优先权	1020100094226 2010-09-29 KR		
其他公开文献	US8432342		
外部链接	Espacenet USPTO		

摘要(译)

一种有机发光显示器的像素，其中所述像素包括：第一晶体管，包括耦合到第一电源的第一电极，第二电极，以及耦合到第一节点的栅电极；第二晶体管，包括耦合到第三电源的第一电极，耦合到第一节点的第二电极，以及耦合到复位控制线的栅电极；第三晶体管，包括耦合到第一节点的第一电极，耦合到第四电源的第二电极，以及栅电极；第四晶体管，包括耦合到第三晶体管的栅电极的第一电极，耦合到扫描线的第二电极，以及耦合到数据线的栅电极；有机发光二极管（OLED）包括耦合到第一晶体管的第二电极的阳极和耦合到第二电源的阴极。

